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(54) Silicon carbide metal diffusion barrier layer

(57) Disclosed is the use of silicon carbide as a barrier layer to prevent the diffusion of metal atoms between adjacent conductors separated by a dielectric material. This advancement allows for the use of low resistivity metals and low dielectric constant dielectric layers in integrated circuits and wiring boards.

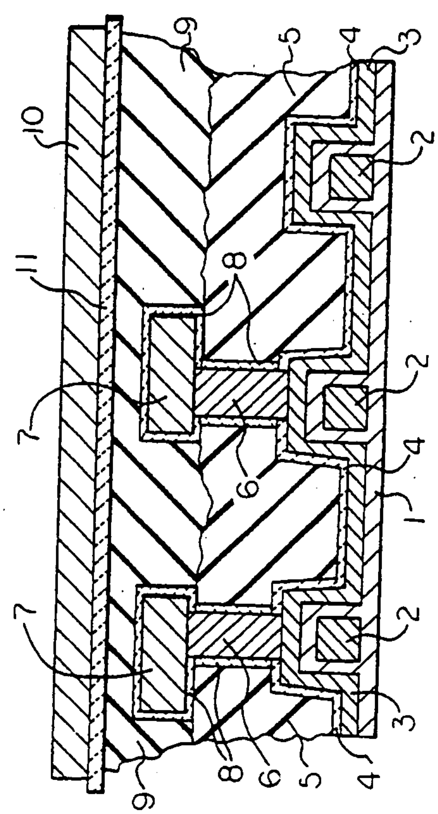

Fig. 1

EP 0 725 440 A2

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Description

The present invention relates to the use of amorphous silicon carbide (a-SiC) films as diffusion barriers in multilevel metal integrated circuit and wiring board designs. The function of the a-SiC is to stop the migration of metal atoms between adjacent conductors which are the device interconnections in the electrical circuit. The reliability added to the circuit by the a-SiC diffusion barrier allows the use of low resistance conductors and low dielectric constant materials as insulation media between the conductors. The combination of the low resistance conductors, the a-SiC diffusion barrier and the low dielectric constant insulation also minimizes the electrical impedance of the circuit. This permits the circuit to operate efficiently from low to high frequencies.

Chiang et al. in "Dielectric Barrier Study for Copper Metallization" (VMIC Conference June 7-8, 1994) discuss the diffusion of copper into silicon nitride, silicon oxynitride and silicon oxide dielectrics. This reference teaches that silicon nitride and silicon oxynitride are much better barriers to metal migration than silicon oxides. The reference, does not, however, discuss the use of silicon carbide as a barrier.

US-A-5,103,285 similarly teaches the use of silicon carbide as a barrier layer between a silicon substrate and a metal wiring layer. The patent does not, however, teach the use of silicon carbide as a diffusion barrier layer between metal wiring and adjacent dielectric layers.

We have now unexpectedly found that silicon carbide forms an excellent barrier layer which prevents the diffusion of low resistance metal conductors into dielectric layers.

An important aspect of the present invention is to provide an improved integrated circuit having greater speed of operation and reliability than are to be found with previously proposed circuits. The circuit of the invention comprises a subassembly of solid state devices formed into a substrate composed of a semiconducting material. The devices within the subassembly are connected by metal wiring formed from high conductivity, low resistance metals. A diffusion barrier layer of amorphous silicon carbide is formed on at least the metal wiring. A dielectric layer is then formed over the silicon carbide layer.

The present invention is based on the unexpected discovery that amorphous silicon carbide will stop the migration of metal atoms between adjacent device interconnections in an electrical circuit. This advance in the art allows IC manufacturers (1) the ability to use high conductivity, low resistance metals (eg., Cu, Ag, Au, alloys and superconductors) as interconnection materials; and (2) the ability to use very low dielectric constant materials as insulating layers between the metal wiring. Without the presence of the a-SiC, the combination of high conductivity metals and low dielectric constant insulating layers suffers from reliability problems such as metal migration and corrosion.

A variety of integrated circuit subassemblies, and a variety of processes for making them, which are known in themselves, may be used in accordance with our invention. Circuits comprising a semiconductor substrate (eg., silicon, gallium arsenide, etc.) having an epitaxial layer grown thereon are exemplary of such circuits. The epitaxial layer is appropriately doped to form the PN-junction regions which constitute the active, solid state device regions of the circuit. These active, device regions are diodes and transistors which form the integrated circuit when appropriately interconnected by metal wiring layers.

Reference is now made to the accompanying drawing, in which Figure 1 is a cross-section of a device of the present invention.

Figure 1 depicts a circuit subassembly (1) having device regions (2) and thin film metal wiring (3) interconnecting the devices.

The metal wiring layers on conventional integrated circuit subassemblies are generally thin films of aluminum. By using the present invention, these thin films can be made of high conductivity metals instead of aluminum. As used herein, high conductivity metals are those having a resistivity below 2.5 microhm-centimeters at 20°C. These include copper, silver, gold, alloys and superconductors.

Methods for depositing such high conductivity metal layers are known in the art. The specific method utilized is not critical. Examples of such processes include various physical vapor deposition (PVD) techniques such as sputtering and electron beam evaporation.

According to the invention, a silicon carbide layer is applied over the metallic wiring layer. Generally, this is accomplished by coating the entire top surface of the circuit subassembly which, obviously, includes the metal wiring. This is depicted as coating (4) in Figure 1. Alternatively, however, the silicon carbide may be selectively applied to the wiring alone by masking, for example, or the entire surface may be coated and then those areas where the silicon carbide is not desired etched away.

Various methods of applying silicon carbide layers are known in the art. Examples of applicable methods include a variety of chemical vapor deposition techniques such as conventional CVD, photochemical vapor deposition, plasma enhanced chemical vapor deposition (PECVD), electron cyclotron resonance (ECR), jet vapor deposition and a variety of physical vapor deposition techniques such as sputtering or electron beam evaporation. These processes involve either the addition of energy (in the form of heat, plasma, etc.) to a vaporized species to cause the desired reaction, or the focusing of energy on a solid sample of the material to cause its deposition.

In conventional chemical vapor deposition, the coating is deposited by passing a stream of the desired precursor gases over a heated substrate. When the precursor gases contact the hot surface, they react and de-

posit the coating. Substrate temperatures in the range of 100-1000°C. are sufficient to form these coatings in several minutes to several hours, depending on the precursors and the thickness of the coating desired. If desired, reactive metals can be used in such a process to facilitate deposition.

In PECVD, the desired precursor gases are reacted by passing them through a plasma field. The reactive species thereby formed are then focused at the substrate where they readily adhere. Generally, the advantage of this process over CVD is that lower substrate temperatures can be used. For instance, substrate temperatures of 50°C. to 600°C. are functional.

The plasma used in such processes comprises energy derived from a variety of sources such as electric discharges, electromagnetic fields in the radio-frequency or microwave range, lasers or particle beams. The use of radio frequency (10 kHz to 10^2 MHz) or microwave (0.1-10 GHz) energy, at moderate power densities (0.1-5 watts/cm^2) is generally preferred in most plasma deposition processes. The specific frequency, power and pressure are, however, generally tailored to the precursor gases and the equipment used.

Examples of suitable precursor gases for use in these processes include (1) mixtures of one or more silanes and/or one or more halosilanes, e.g., trichlorosilane, with one or more alkanes of one to six carbon atoms, e.g., methane, ethane or propane; (2) an alkylsilane such as methylsilane, dimethylsilane or trimethylsilane; or (3) a silacyclobutane or disilacyclobutane as described in US-A-5,011,706.

The plasma enhanced chemical vapor deposition of trimethylsilane is especially preferred for the purposes of this invention.

After the silicon carbide has been deposited, a dielectric layer is then applied over the silicon carbide layer. This is shown as interlevel dielectric layer (5) in Figure 1. The specific dielectric layer and the method for its deposition are not critical to the invention. By using our process, however, one can utilize low dielectric constant (DK) layers. As used herein, low dielectric constant layers are those with a DK of less than 3.5.

Examples of suitable dielectric materials include silicon oxides, silicon nitrides, silicon oxynitrides, silicon carbides, silicon oxycarbides, silicon carbonitrides and organic materials such as silicones, polyimides, epoxy compounds or thermoplastic film polymers based on para-xylylene [PARYLENE™ - see also the definition of "parylene" in The Condensed Chemical Dictionary, Eighth Edition, Van Nostrand Reinhold Company, New York, p 660]. Obviously, more than one layer of these dielectrics may be used.

The techniques for applying these coatings are also known in the art. They include spin-on processes, conventional CVD, photochemical vapor deposition, plasma enhanced chemical vapor deposition (PECVD), electron cyclotron resonance (ECR), jet vapor deposition and a variety of physical vapor deposition techniques such as sputtering and electron beam evaporation.

The preferred process of the present invention comprises applying an hydridosiloxane resin having units of the structure $HSi(OH)_x(OR)_yO_{z/2}$ in which each R is, independently, an organic group which, when bonded to silicon through the oxygen atom, forms an hydrolysable substituent, $\underline{x}$ = 0-2, $\underline{y}$ = 0-2, $\underline{z}$ = 1-3 and $\underline{x} + \underline{y} + \underline{z} = 3$. These resins may either be fully condensed ($\underline{x}$ = 0, $\underline{y}$ = 0 and $\underline{z}$ = 3) or be only partially hydrolysed ($\underline{y}$ does not equal 0 over all the units of the polymer) and/or partially condensed ($\underline{x}$ does not equal 0 over all the units of the polymer).

Although not represented by this structure, various units of these resins may have either zero or more than one Si-H bond due to various factors involved in their formation and handling.

Exemplary of these resins are those formed by the processes of US-A-3,615,272; US-A-5,010,159 US-A-4,999,397 and US-A-5,063,267. These resins are applied by a spin-on process followed by heating to convert them to a ceramic.

If desired for a multilayer device, one can form another layer of metal wiring on the dielectric layer, and then interconnect the layers by etching through the dielectric and the silicon carbide layers. Figure 1 shows such a second metal wiring layer (7) which is interconnected with selected regions of the first layer of wiring by interconnects (6). Again, however, if the wiring is to be a high conductivity material, a layer of silicon carbide (8) should be deposited between the dielectric and the metal to prevent diffusion of the metal into the dielectric. This silicon carbide layer can be formed as described above. In such a manner, the metal wiring is sandwiched between layers of silicon carbide. This process can be repeated many times for the various layers of metallization within a circuit. Figure 1, for example, shows a second layer of dielectric (9), and a third layer of wiring (10) protected by a third layer of silicon carbide (11).

It should be noted that silicon carbide with a low dielectric constant (e.g., DK < 5) may also replace the dielectric layer (i.e., layers 5 and 9 in Figure 1). In this embodiment, one would merely form a layer of silicon carbide over a metal wiring layer as described above, and then form another metal layer on the silicon carbide.

It should also be noted that this technology can be applied to the wiring boards onto which the above circuits are mounted. The structures of the metal wiring and dielectric layers on these wiring boards would be the same as those described above.

Claims

1. An integrated circuit comprising:

A) a circuit subassembly comprising a semiconductor substrate having solid state device

regions and, deposed on the surface of the semiconductor substrate, metal wiring interconnecting the solid state device regions, the metal wiring having a resistivity of less than 2.5 microhm-centimeters;
B) an amorphous silicon carbide layer covering at least the metal wiring; and
C) a dielectric layer covering at least the silicon carbide layer.

2. The integrated circuit of claim 1, wherein the amorphous silicon carbide covers the metal wiring and the surface of the circuit subassembly containing the device regions.

3. The integrated circuit of claim 1 or claim 2 wherein the dielectric layer is selected from silicon oxides, silicon nitrides, silicon oxynitrides, silicon carbides, silicon oxycarbides, silicon carbonitrides and organic materials.

4. The integrated circuit of any of claims 1 to 3, wherein the dielectric layer has a dielectric constant of less than 3.5.

5. The integrated circuit of any of claims 1 to 4, wherein the dielectric layer is a silicon oxide.

6. The integrated circuit of any of claims 1 to 5, wherein the metal wiring is thin film metal wiring.

7. The integrated circuit of any of claims 1 to 6, wherein the metal wiring is selected from copper, silver, gold, alloys and superconductors.

8. The integrated circuit of any of claims 1 to 7, further comprising a second amorphous silicon carbide layer covering the dielectric layer.

9. The integrated circuit of claim 8, further comprising a second layer of metal wiring formed on the second layer of silicon carbide, wherein the second layer of metal wiring is electrically connected to the first layer of metal wiring.

10. A wiring board comprising:

A) a wiring board subassembly containing thereon metal wiring having a resistivity below 2.5 microhm-centimeters;
B) an amorphous silicon carbide layer covering the metal wiring; and
C) a dielectric layer covering the silicon carbide layer.

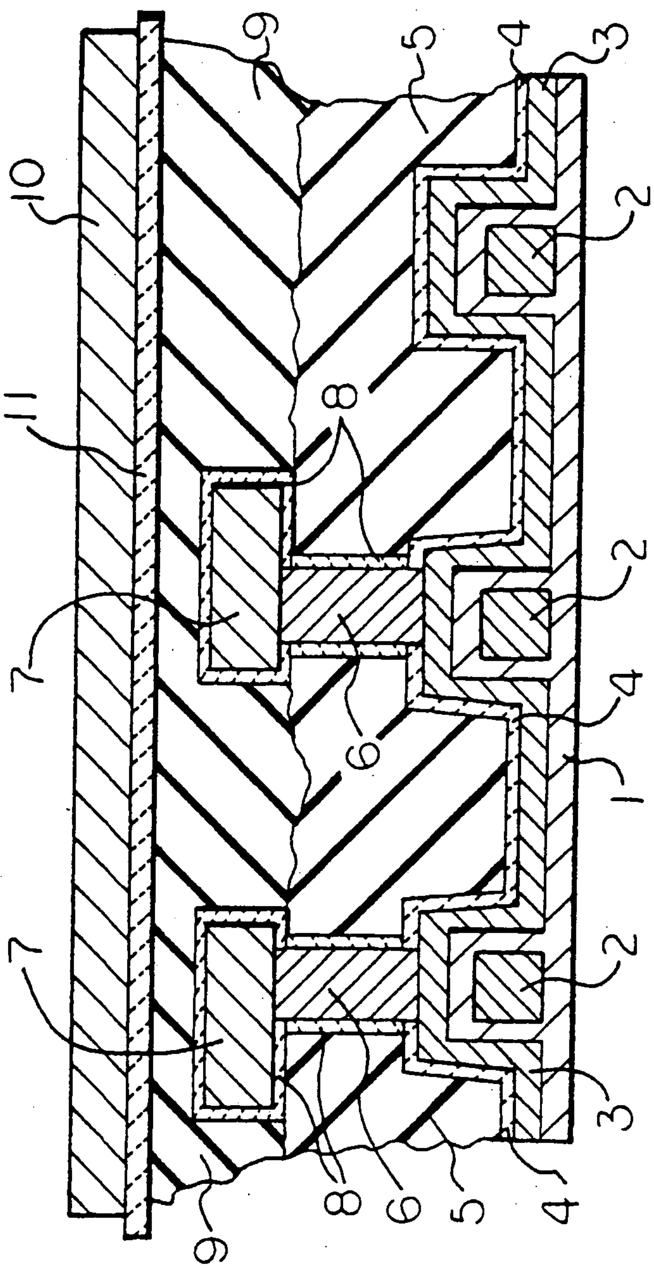

Fig. 1